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(54) NROM cell with generally decoupled primary and secondary injection

(57) A method of creating a nitride, programmable read only memory (NROM) cell includes the step of decoupling injection of channel hot electrons into a charge trapping layer of the NROM cell from injection of non-channel electrons into the charge trapping layer. The step of decoupling can include the step of minimizing the injection of the non-channel electrons into the charge trapping layer. Alternatively, it includes the step of minimizing the generation of the non-channel electrons. The present invention includes cells which have minimal injection of non-channel electrons therein.

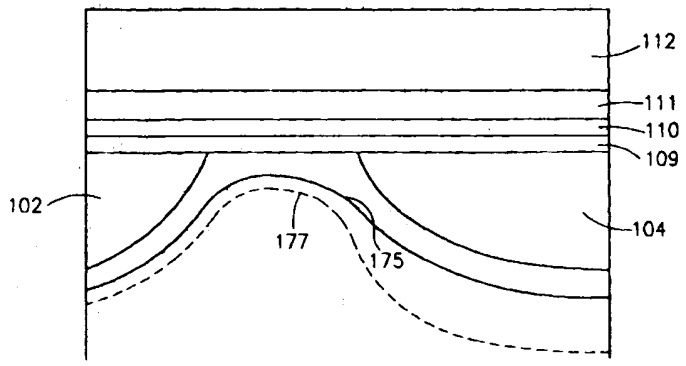

FIG.6C

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to FLASH, electrically erasable, programmable read only memory (EEPROM) and nitride, programmable read only memory (NROM) cells in general and to secondary injection therein in particular.

BACKGROUND OF THE INVENTION

[0002] Floating gate memory cells are used for electrically erasable, programmable read only memory (EEPROM) and Flash EEPROM cells. As shown in Fig. 1 to which reference is now made, floating gate cells comprise source and drain portions 102 and 104 embedded in a substrate 105, between which is a channel 100. A floating gate 101 is located above but insulated from channel 100 and a gate 112 is located above but insulated from floating gate 101.

[0003] For most floating gate cells, the standard electron injection mechanism (for programming) is channel hot electron injection, in which the source to drain potential drop creates a lateral field that accelerates channel electrons e_1 from source 102 to drain 104. This is indicated by arrow 10. Near drain 104, a vertical field created by the gate voltage allows hot channel electrons e_1 to be injected (arrow 12) into floating gate 101.

[0004] There is another injection mechanism, known as "secondary electron injection". As indicated by arrow 14, some of the channel electrons e_1 create hole and electron pairs through ionization of valence electrons in channel 100 or drain 104. The probability of the ionization is labeled M_1 and it indicates the ratio between the channel current and the hole substrate current.

[0005] Due to the positive potential of drain 104, generated electron e_2 is collected (arrow 16) by drain 104. However, as indicated by arrow 18, hole h_2 accelerates towards the low substrate potential of substrate 105. On the way, another impact ionization event may occur, creating another electron-hole pair e_3 - h_3, with probability M_2. Hole h_3 is pulled (arrow 20) further into substrate 105 and is of no concern. However, electron e_3 (known as the "secondary electron") is accelerated (arrow 22) toward positive gate 112 where, if it has gained sufficient energy, it is injected into floating gate 101. The probability of this occurring is labeled T.

[0006] The current for secondary injection is defined as:

$$I_g = I_{ds} * M_1 * M_2 * T$$

where I_{ds} is the channel current from source to drain.

[0007] Because this current is significant, some floating gate devices have been built to enhance it, thereby reducing programming time and programming voltages. The following articles discuss some possible methods to enhance the secondary injection:

J. D. Bude, et al., "Secondary Electron Flash - a High Performance, Low Power Flash Technology for 0.35µm and Below", IEDM 97, pp. 279 - 282;

J. D. Bude, et al., "EEPROM/Flash Sub 3.0V Drain-Source Bias Hot Carrier Writing", IEDM 95, pp. 989 - 992; and

J. D. Bude and M. R. Pinto, "Modeling Nonequilibrium Hot Carrier Device Effects", Conference of Insulator Specialists of Europe, Sweden, June 1997. These references enhance the secondary generation and injection in two ways as shown in Figs. 2A and 2B to which reference is now made, by implanting (Fig. 2A) substrate 105 with Boron pockets 116 and by applying a negative substrate bias V_B to substrate 105 (Fig. 2B).

[0008] Boron pockets 116 (Fig. 2A), when implanted with relatively high energy, enhance the field in the substrate and hence, enhance the probability M_2 of secondary generation. This higher Boron concentration is effective also in accelerating secondary electrons and hence, enhances their probability T of injection.

[0009] The potential drop V_{db} from drain 104 to substrate 105 is larger by 1V than the potential drop V_{ds} from drain to source due to the built-in potential in the n+ / p- substrate junction. This enhances both the probability M_2 of a secondary impact and the probability T of injection. To further enhance secondary injection, a negative substrate bias V_B can be applied, as shown in Fig. 2B.

[0010] It will be appreciated that the energy balance for secondary injection is a function of the drain voltage V_d (which defines the voltage in the channel), the built-in potential V_{bi}, the substrate voltage V_{sub} and the energy De_{sec} after impact ionization. This compares to the primary electron injection mechanism (of channel hot electron injection) which is a function of the drain to source voltage V_{ds}.

[0011] Typically, if the drain to source voltage V_{ds} is of 3V and the substrate voltage is at 0V, the primary electrons are accelerated by 3V while the secondary electrons are accelerated by 4V. If the substrate voltage is decreased to -1V, then the secondary electrons are accelerated by 5V. Thus, applying negative voltage to the substrate increases the secondary injection mechanism. This is illustrated in Fig. 2B which shows the potential energy across channel 100 (from drain 104 (at point A) to source 102 (point B) and into the substrate 105 (point C is at the electrode of substrate voltage V_b). In Fig. 2B, the drain / source voltage V_{ds} is 3V, the gate / source voltage V_{gs} is 2V and the channel length is 0.25µm.

[0012] The solid line, labeled 120, indicates the

potential energy in a standard situation where source / substrate voltage V_{bs} is 0.0V. The potential energy drops from drain 104 to source 102 and then increases into substrate 105. Thus, the total potential drop from drain (point A) to substrate (point C) is about 1eV higher than that of the drain to source (point A to point B). A generated hole h_2 will escape the drain 104 and will create a secondary electron e_3 with energy of about 0.2 - 0.7eV.

[0013] This energy, when combined with the acceleration of secondary electron e_3 over several volts of substrate to channel potential towards gate 112, makes the probability of injection T of secondary electron e_3 higher than that of primary electron e_1. However, there are many more primary electrons e_1 available than secondary electrons e_3 and thus, most of the injection remains the primary electrons e_1. Since the injected electrons (primary and secondary) spread out in floating gate 101, there is no way to tell where injection occurred.

[0014] When the source / substrate voltage V_{bs} is decreased to -1.0V, shown with the dashed line 122, the potential energy into substrate 105 increases, although the potential energy in the drain and across the channel does not change. The increased substrate potential provides additional energy to secondary electrons e_3 while not affecting the energy of channel electrons e_1.

[0015] Secondary injection adds to the primary injection mechanism to provide a faster and/or lower voltage injection into a floating gate cell. Unfortunately, secondary injection is not good for all types of cells. There are some cells, such as nitride, programmable read only memory (NROM) cells, for which enhancing secondary injection appears not to enhance the operation of the cell.

[0016] NROM cells are described in Applicant's copending US patent application 08/905,286, entitled "Two Bit Non-Volatile Electrically Erasable And Programmable Semiconductor Memory Cell Utilizing Asymmetrical Charge Trapping" which was filed August 1, 1997. The disclosure of the above-identified application is incorporated herein by reference.

[0017] Figs. 3A, 3B and 3C, to which reference is now made, schematically illustrate the dual bit NROM cell. Similar to the floating gate cell of Fig. 1, the NROM cell has channel 100 between two bit lines 102 and 104 but, unlike the floating gate cell, the NROM cell has two separated and separately chargeable areas 106 and 108. Each area defines one bit. For the dual bit cell of Figs. 3, the separately chargeable areas 106 and 108 are found within a nitride layer 110 formed in an oxide-nitride-oxide (ONO) sandwich (layers 109, 110 and 111) underneath gate 112.

[0018] To read the left bit, stored in area 106, right bit line 104 is the drain and left bit line 102 is the source. This is known as the "read through" direction, indicated by arrow 113. To read the right bit, stored in area 108, the cell is read in the opposite direction (a "reverse read"), indicated by arrow 114. Thus, left bit line 102 is the drain and right bit line 104 is the source.

[0019] Fig. 3B generally indicates what occurs within the cell during reading of the left bit of area 106. An analogous operation occurs when reading the right bit of area 108.

[0020] To read the left bit in area 106, the left bit line 102 receives the source voltage level V_s, typically on the order of 0V, and the right bit line 104 receives the drain voltage V_d, typically of 1 - 2V. The gate 112 receives a relatively low voltage V_g, which typically is a low voltage of 2.5 - 3V.

[0021] The presence of the gate and drain voltages V_g and V_d, respectively, induce a depletion layer 54 and an inversion layer 52 in the center of channel 100. The drain voltage V_d is large enough to induce a depletion region 55 near drain 104 which extends to the depletion layer 54 of channel 100. This is known as "barrier lowering" and it causes "punch-through" of electrons from the inversion layer 52 to the drain 104. The punch-through current is only minimally controlled by the presence of charge in right area 108 and thus, the left bit can be read irrespective of the presence or absence of charge in right area 108.

[0022] Since area 106 is near left bit line 102 which, for this case, acts as the source (i.e. low voltage level), the charge state of area 106 will determine whether or not the inversion layer 52 is extended to the source 102. If electrons are trapped in left area 106, then the voltage thereacross will not be sufficient to extend inversion layer 52 to the source 102 and a "0" will be read. The opposite is true if area 106 has no charge.

[0023] For NROM cells, each bit is programmed in the direction opposite that of its reading direction. Thus, to program left bit in area 106, left bit line 102 receives the high programming voltage (i.e. is the drain) and right bit line 104 is grounded (i.e. is the source). This is shown in Fig. 3C. The opposite is true for programming area 108.

[0024] The bits are erased in the same directions that they are programmed. However, for erasure, a negative erasure voltage is provided to the gate 112 and a positive voltage is provided to the bit line which is to be the drain. Thus, to erase the charge in left area 106, the erase voltage is provided to left bit line 102. The highly negative erase voltage creates holes in the n+ junction (near left bit line 102) through band-to-band tunneling. These holes are accelerated by the lateral field near the drain (left bit line 102) and the ONO surface. Some holes gain enough energy to be injected through the bottom oxide 109 in a process known as "tunnel assisted hot hole injection".

[0025] Typically, programming and erasure are performed with pulses of voltage on the drain and on the gate. After each pulse, a verify operation occurs in which the threshold voltage level of the cell (i.e. the gate voltage level at which the cell becomes significantly conductive) is measured. During programming, the

threshold voltage level Vtp is steadily increased until the cell will not pass any significant current during a read operation. During erasure, the opposite is true; the threshold voltage level Vte is decreased until a significant current is present in the cell during reading. Should the cell not meet the erase specification (typically defined by a maximum number of pulses to achieve erasure), it is no longer considered functional.

[0026] The enhancements for secondary injection are indirectly implemented in the NROM cell as well. In some arrays, the NROM cell has an inherent back bias, due to voltage drops in the array. This results in a positive source voltage V_s, which requires a higher drain voltage V_d to meet the required drain-to-source voltage V_{ds} for a desired programming speed. As discussed hereinabove with respect to Fig. 2, the increased drain voltage V_d enhances the secondary injection since the drain to bulk potential is increased accordingly. And, since the source voltage V_s is more positive than desired, the drain-to-source voltage V_{ds} is lower than desired which, in turn, reduces the drive for the primary injection mechanism. Unfortunately, as indicated in Figs. 4A and 4B, to which reference is now made, the secondary injection effect degrades the operation of the NROM cell.

[0027] Figs. 4A and 4B illustrate the results of an experiment where one of the bits was programmed and then erased, once with substrate 105 at 0V and once with substrate 105 at -2V. The remaining voltages stayed the same. If programming occurred properly, then the programmed bit should change threshold voltage during programming, while the unprogrammed bit should not change at all, If programming occurred properly, then during erasure, the threshold voltage of the programmed bit should quickly return to the unprogrammed level.

[0028] In Fig. 4A, the threshold voltage is graphed against the programming time. Programming ends when the threshold level of the bit being programmed has increased by 2.0V.

[0029] Curves 134 and 136 show the results for programming with the standard source / substrate voltage V_{sb} of 0.0V, for the bit being programmed and the unprogrammed bit, respectively. As can be seen in curve 134, the threshold level of the bit being programmed increases steadily until, at 100µsec, the bit reaches the programmed level. At the same time, the voltage level of the unprogrammed bit increases to slightly above 0.2V (curve 136).

[0030] Curves 138 and 140 show the results for programming with the negative source / substrate voltage V_{sb} of -2V, for the bit being programmed and the unprogrammed bit, respectively. In curve 138, the threshold level of the bit being programmed increases faster and becomes programmed by 10µsec. At the same time, the voltage level of the unprogrammed bit (curve 140) grows to 0.5V. This threshold level reduces the operating window for two bits. In other words, the punchthrough read of one bit is affected by the information in the other bit.

[0031] In Fig. 4B, the threshold voltage is graphed against the erase time. Curves 144 and 146 show the results for erasure of the bit programmed with the standard source / substrate voltage V_{sb} of 0.0V, for the programmed and unprogrammed bits, respectively. The threshold level of the programmed bit drops sharply (curve 144) until, at 1.0sec, the bit is unprogrammed. At the same time, the voltage level of the unprogrammed bit drops back to 0.0V (curve 146)

[0032] Curves 148 and 150 show the results for erasure of the bit programmed with the negative source / substrate voltage V_{sb} of -2V, for the programmed and unprogrammed bits, respectively. The unprogrammed bit is further erased, back to almost 0.0V. However, the programmed bit erases slowly and still has a significant threshold voltage level even after 1.0sec of erasure.

[0033] Thus, using a negative substrate voltage V_B, whether to solve a back bias or to enhance secondary injection for NROM cells, does not improve their performance. To the contrary, it greatly degrades their performance. Similarly, adding a pocket implant improves their primary performance but may adversely affect their endurance by enhancing the secondary injection.

[0034] US Serial Numbers 09/082,280 and 09/413,408, assigned to the common assignees of the present invention and incorporated herein by reference, describe using pocket implants, such as enhance primary injection, in an NROM cell to shape the lateral field such that charge is injected in an area from which it can be erased. This dramatically improves the operation of the cell with respect to the primary injection.

SUMMARY OF THE INVENTION

[0035] Applicant has realized that the secondary injection reduces the performance of NROM cells. Furthermore, as will be described in more detail hereinbelow, Applicant has realized that the cause is the secondary electrons that are injected far from the bit line junctions. These secondary electrons are not removable during erasure and thus, reduce the ability of the NROM cell to separate between the two charge areas.

[0036] Therefore, the present invention seeks to decouple the primary injection mechanism from other injection mechanisms, like the secondary one, enhancing the primary mechanism while reducing the other injection mechanisms.

[0037] There is therefore provided, in accordance with a preferred embodiment of the present invention, a method of creating a nitride, programmable read only memory (NROM) cell includes the step of decoupling injection of channel hot electrons into a charge trapping layer of the NROM cell from injection of non-channel electrons into the charge trapping layer. The step of decoupling can include the step of minimizing the injection of the non-channel electrons into the charge trap-

ping layer. Alternatively, it includes the step of minimizing the generation of the non-channel electrons.

[0038] Additionally, in accordance with a preferred embodiment of the present invention, the step of injection minimization includes at least one of the following steps: minimizing the concentration of Boron deep in the substrate, implanting a shallow threshold voltage implant, implanting deep bit lines and making the channel to be shorter than a standard length.

[0039] Furthermore, in accordance with a preferred embodiment of the present invention, the NROM cell has at least one Boron pocket implants and the step of Boron concentration reduction includes the step of implanting Arsenic or Phosphorous pocket implants deeper than the Boron pocket implants.

[0040] Still further, in accordance with a preferred embodiment of the present invention, the threshold voltage implant step includes the step of implanting two threshold voltage implants, a first surface implant of Boron and a second deeper implant of Arsenic or Phosphorous. Additionally, Boron pockets can be implanted.

[0041] Additionally, in accordance with a preferred embodiment of the present invention, the step of generation minimization includes at least one of the following steps: minimizing the concentration of Boron deep in the substrate, implanting a shallow threshold voltage implant and making the channel to be shorter than a standard length.

[0042] Alternatively, in accordance with a preferred embodiment of the present invention, the NROM cell can include a shallow threshold voltage implant at least of Boron into the channel. The concentration of the Boron is reduced by a factor of 2 at least a distance of 10 - 20, 20 - 30, 30 -4 0 and 50 - 100nm from a surface of the channel.

[0043] Moreover, in accordance with a preferred embodiment of the present invention, the shallow threshold implant has a first implant of Boron and a counterdoping implant of one of Arsenic and Phosphorous, wherein the counterdoping implant is deeper in the channel than the first implant.

[0044] Further, in accordance with a preferred embodiment of the present invention, the cell also includes a pocket implant near at least one of the bit lines.

[0045] In accordance with a further preferred embodiment of the present invention, the NROM cell can include a double pocket implant near at least one of the bit lines wherein the double pocket implant is formed of two pocket implants, a p+ implant near a surface of the substrate and an n- implant below the p+ implant.

[0046] In accordance with a still further preferred embodiment of the present invention, the NROM cell can include a substrate having two bit lines and a channel therebetween, wherein the channel is no longer than 0.2μm, and an ONO layer at least above the channel.

[0047] Further, in accordance with a preferred embodiment of the present invention, the channel is no longer than 0.15μm. Alternatively, it is no longer than 0.1μm.

[0048] Moreover, in accordance with a preferred embodiment of the present invention, the NROM cell can include a substrate having two bit lines and a channel therebetween, wherein the bit lines have a depth of no less than 0.3μm into the substrate, and an ONO layer at least above the channel.

[0049] There is also provided, in accordance with a preferred embodiment of the present invention, a method of creating nitride, programmable read only memory cell, the method comprising the steps of having a high ratio of surface injection to deep injection of electrons into a charge trapping layer of the NROM cell.

[0050] Moreover, in accordance with a preferred embodiment of the present invention, the NROM cell has at least Boron pocket implants and the method includes at least one of the following steps: implanting a shallow threshold voltage implant, implanting pocket implants of one of Arsenic and Phosphorous deeper than the Boron pocket implants or implanting two threshold voltage implants, a first surface implant of Boron and a second deeper implant of one of Arsenic and Phosphorous.

[0051] There is further provided, in accordance with a preferred embodiment of the present invention, a method of creating a nitride, programmable read only memory (NROM) cell, comprising the steps of generating a zero substrate potential at a distance no less than 45 - 55nm into said substrate.

[0052] Additionally, in accordance with a preferred embodiment of the present invention, the step of generating includes the steps of minimizing the concentration of Boron deep in the substrate by implanting pocket implants of one of Arsenic and Phosphorous deeper than said Boron pocket implants, implanting two threshold voltage implants, a first surface implant of Boron and a second deeper implant of one of Arsenic and Phosphorous or implanting a shallow threshold voltage implant with or without Boron pockets.

[0053] Moreover, in accordance with a preferred embodiment of the present invention, the NROM cell has a channel and the step of generation includes the step of making the channel to be shorter than a standard length.

[0054] Finally, there is provided, in accordance with a preferred embodiment of the present invention, a method of operating a nitride, programmable read only memory (NROM) cell to have minimum injection from non-channel electrons. The cell has bit lines serving as source and drain to the cell and the method includes the step of providing the lowest source voltage Vs which provides a desired drain to source voltage V_{ds} to the cell.

BRIEF DESCRIPTION OF THE DRAWINGS

[0055] The present invention will be understood

and appreciated more fully from the following detailed description taken in conjunction with the appended drawings in which:

Fig. 1 is a schematic illustration of a secondary injection within a floating gate cell;
Fig. 2A is a schematic illustration of the cell of Fig. 1 with pocket implants;
Fig. 2B is a graphical illustration of potential drops within the floating gate cell;
Figs. 3A, 3B and 3C are schematic illustrations of the operation of a prior art dual bit, nitride programmable read only memory (NROM) cell;
Figs. 4A and 4B are graphical illustrations of the threshold voltage during conventional programming and erasure, respectively, of the NROM cell;
Figs. 5A and 5B are schematic illustrations of the state of the NROM cell of the prior art after the first cycle of programming and erasure, respectively;
Figs. 5C and 5D are schematic illustrations of the state of the NROM cell of the prior art after the $20{,}000^{th}$ cycle of programming and erasure, respectively;
Fig. 6A is a graphical illustration of Boron concentration for a cell of the present invention and of the prior art;
Fig. 6B is a band diagram illustration for the cells whose Boron concentrations are shown in Fig. 6A;
Fig. 6C is a schematic illustration of the depletion layers for the cells whose Boron concentrations are shown in Fig. 6A;
Figs. 7A and 7B are graphical illustrations of the threshold voltage during programming and erasure, respectively, for the cells whose Boron concentrations are shown in Fig. 6A;
Fig. 8 is a flow chart illustration of a standard process for producing an NROM cell;
Fig. 9 is a schematic illustration of an NROM cell having a double pocket, where the second pocket implant reduces the depth of the first pocket implant;
Fig. 10A is a schematic illustration of an NROM cell having a shallow threshold voltage implant;
Fig. 10B is a schematic illustration of an NROM cell having a double threshold voltage implant;
Fig. 10C is a schematic illustration of an NROM cell having a shallow threshold voltage implant and a pocket implant; and
Figs. 11A and 11B are schematic illustrations of an NROM cell having deep junctions and a short channel length, respectively.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0056] Applicant has realized that secondary electrons that are injected far from the bit line junctions cause early failure of the NROM cells. As described hereinbelow with respect to Figs. 5, these secondary electrons are not removable during erasure and thus, they reduce the ability of the NROM cell to withstand a large number of program and erase cycles.

[0057] Reference is now made to Figs. 5A, 5B, 5C and 5D, which show the charge stored in right area 108 (Figs. 3) of the nitride layer as a function of distance along the channel for one cell. Figs. 5 show only the charge over the channel region as this is the only charge which affects the threshold voltage V_t of the device.

[0058] Fig. 5A shows that, after the first cycle of programming, a significant amount of charge, labeled 151, is stored close to the right bit line, which, in this example, is the drain for programming and erasure. As one moves away from the drain, the amount of charge reduces, eventually to zero. Fig. 5B shows the amount of charge, labeled 152, left after the first erase cycle. The erase electric field is typically so effective that it removes extra electrons (more than were present in charge 151) such that section 152 is positive while section 151 is negative. Section 152 is thus, hatched, to indicate that it is positively charged.

[0059] Figs. 5C and 5D parallel Figs. 5A and 5B, respectively, but for after 20,000 cycles. After programming, there is a significant charge, labeled 154, close to the drain, as in Fig. 5A but with less electrons. However, there is also another section of charge, labeled 156, further from the drain, which was injected far from the drain junction and was not erased during previous erase cycles. After the $20{,}000^{th}$ erase cycle, extra section 156 still remains and is negatively charged, though the previously programmed section 154 has become positively charged section 158 (Fig. 5D).

[0060] As can be understood from the above discussion, the charge, in section 156, is not erased during erasure operations and remains trapped there. Trapped charge 156 acts as partially programmed charge. It is due to trapped charge 156 that, at the $20{,}000^{th}$ cycle, fewer programming pulses are required to achieve the programmed threshold voltage level (since the bit is already, in effect, partially programmed).

[0061] Furthermore, the accumulation of trapped negative charge 156 far from the junction increases the threshold voltage level, which affects the reverse read. The erase operation compensates by accumulating extra positive charge (in the form of holes) close to the junction, which makes the erase time take longer. Another problem with hole compensation for non-erased charge is the large dipole field that exists between the hole and the electron distributions. Holes move toward electrons at high temperatures and recombine with the electrons during any retention bake. This movement of holes under high field and temperature into the channel reduces the programming threshold. In response, the programming threshold voltage V_{tp} is increased to compensate. However, this, in turn, reduces the reliability margin of the part.

[0062] US 09/082,280 and US 09/413,408 attempt to solve the problem of trapped charge 156 for primary injection, but both can be further improved. US 09/082,280 reduces the field far from the junctions and ensures that a high field is found near the bit line junction only. US 09/413,408 self-aligns the areas of hot electron injection (programming) and hot hole injection (erasure). Both applications function to increase the primary, channel hot hole injection mechanism. However, as Applicant has realized, neither method is successful in resolving the above problem since neither method reduces the secondary injection mechanism.

[0063] The secondary injection mechanism causes some trapped charge 156 to be generated with each programming cycle. Even if most of the secondary electrons are removed with each cycle, over many cycles, there will be a slow increase in the size of remaining trapped charge 156, which, eventually, will degrade the cell.

[0064] As described in the Background, the NROM cell uses the punchthrough effect to read only one of the two bits. Punchthrough occurs under the bit not being read and is dependent on the width of the trapped charge. Punchthrough can only occur if the charged area is narrow. Thus, if the presence of remaining trapped charge 156 widens the total area of trapped charge, punchthrough will become less and less effective, until the erase state of the other bit cannot be recognized and the part will fail.

[0065] The present invention seeks to decouple the primary injection mechanism from the secondary one, emphasizing the primary mechanism while reducing the secondary one.

[0066] Applicant has realized that the secondary electrons are mainly produced deep in substrate 105 while primary electrons are produced near the surface of substrate 105. Therefore, in accordance with a preferred embodiment of the present invention, the two processes are decoupled, by affecting either the generation of the secondary electrons or by affecting the injection efficiency T. Another option is to enhance the primary injection while not enhancing the secondary injection. In other words, the present invention improves the ratio of the primary to secondary injections.

[0067] Reference is now made to Figs. 6A, 6B and 6C, which illustrate the general principles of the present invention and to Figs. 7A and 7B, which illustrate the results for the experiment discussed with respect to Figs. 6A and 6B, but for an array of the present invention.

[0068] Fig. 6A is a graph of the Boron concentration into substrate 105. Two graphs 170 and 172 are shown which indicate the Boron concentration of the present invention and of a prior art cell having a standard pocket implant, respectively. For the present invention, (graph 170), the Boron concentration is significantly reduced at about 0.5μm from the SiO_2 surface. Otherwise (graph 172), the Boron concentration decreases only further than 1μm from the SiO_2 surface. With the present invention, fewer secondary electrons will be generated because there is little or no Boron in the areas where secondary electron generation occurs.

[0069] Fig. 6B is a band diagram corresponding to the Boron concentrations of Fig. 6A. Fig. 6B shows valence bands 173A and 173B and conduction bands 176A and 176B for the cell of the present invention vs. the prior art cell. As can be seen, the bands 173A and 176A for the present invention have lower slopes, far from surface 171, than do the bands 173B and 176B for the prior art. Since the slope of the bands indicates the fields found at those locations, it can be seen that, for the present invention, the fields are reduced deep into the substrate 105. Thus, there are lower fields in the areas where secondary electrons are produced and thus, the probability that secondary injection will occur has been reduced.

[0070] In effect, the substrate potential (the point where the substrate potential is 0V) has been moved further into the substrate. Point A, the substrate potential for the present invention, is farther from surface 171 than point B, the substrate potential for the prior art. This provides at least a three order of magnitude improvement in

[0071] Fig. 6C is an illustration of the depletion region of the cell for the prior art cell (solid line 175) and the present invention (dashed line 177). As can be seen, depletion region 177 is approximately the same as depletion region 175 in the channel but much deeper than depletion region 175 near drain 104. Since the strength of the vertical field is an inverse function of the distance of the edge of the depletion region from the drain, the vertical field deep in the substrate is much lower in the present invention than in the prior art.

[0072] Figs. 7A and 7B graph the threshold voltage during programming and erasure, respectively, for the experiment discussed with respect to Figs. 4A and 4B, but for an array of the present invention. Four curves are shown in each figure.

[0073] For Fig. 7A, curves 174 and 176 show the results for programming with the standard source / substrate voltage V_{sb} of 0.0V, for the bit being programmed and the unprogrammed bit, respectively. Curves 178 and 180 show the results for programming with the reduced source / substrate voltage V_{sb} of -2V, for the bit being programmed and the unprogrammed bit, respectively.

[0074] As can be seen in curve 174, programming is finished by 20μsec, which is five times faster than the 100μsec of curve 134 (Fig. 4A). Furthermore, the voltage level of the unprogrammed bit hardly increases (curve 176). With the negative source / substrate voltage V_{sb}, the bit being programmed (curve 178) becomes programmed by 5μsec and, once again, the voltage level of the unprogrammed bit (curve 180) hardly increases. In other words, less far-from-the-junction secondary electrons are being injected.

[0075] In Fig. 7B, the threshold voltage is graphed against the erase time. Curves 184 and 186 show the results for erasure of the bit programmed with the standard source / substrate voltage V_{sb} of 0.0V, for the programmed and unprogrammed bits, respectively, while curves 188 and 190 show the results for programming with the negative source / substrate voltage V_{sb} of -2V. For both programmed bits (curves 188 and 184), the threshold voltage drops significantly such that, by 1 sec, both bits are erased. Similarly, the unprogrammed bits are slightly erased as well.

[0076] Figs. 7A and 76 indicate that, with the reduced deep Boron concentration, the trapped charge 156 is sufficiently reduced such that the dual bit NROM cell operates as expected, with two, separately programmable and separately erasable bits.

[0077] In the following, various embodiments of cells whose ratio of primary to secondary injection is improved are provided, as is one process flow for creating each embodiment. In order to understand the process flows, a general process flow is first provided, in Fig. 8, to which reference is now made.

[0078] The process is based on that described in US Serial Number 09/082,280 and will be provided here without significant explanation.

[0079] The process begins, in step 190, with the steps of a standard CMOS (complementary metal oxide semiconductor) front end, followed by deposition (step 191) of the ONO layer. The CMOS front end steps include field isolation, sacrificial oxide and the n-channel and n-well implants. The ONO deposition is described in US Serial Number 09/082,280.

[0080] Step 192 is a bit line (BL) mask step in which the mask that defines the bit lines is laid down on substrate 105. The oxide and nitride layers are etched using this mask. The Boron is then implanted in two pocket implant steps (step 193), as described in US 09/082,280, with angled implants, producing Boron pockets 116. The implant has a dosage of $1.5x10^{13}$ per cm^2 at 60Kev and at an angle of 25° to the right and left of vertical.

[0081] In step 194, the bit lines are implanted, with a dosage of $3x10^{15}$ per cm^2 at 45Kev and at an angle of 7° parallel to the bit line mask, after which, in step 195, the bit line mask is removed.

[0082] In step 196, the bit lines are oxidized, if desired, after which an array protect mask is laid down (step 197) and the ONO is removed from the periphery of the chip (i.e. from everywhere but the array). With the array protect mask in place, the standard CMOS operations for producing high and low voltage transistors in the periphery are performed (step 198).

[0083] A gate oxide, for the high voltage (HV) transistors, is now grown (step 199) after which, a threshold adjust implant, which is typically a blanket, high voltage boron implant, is performed (step 200).

[0084] A high voltage mask is laid down (step 201) and the high voltage oxide is etched (step 202). A low voltage Boron implant is performed (step 203) after which, the high voltage mask is removed (step 204). This is followed by a low voltage gate oxide growth (step 205) and a polysilicon and silicide deposition (step 206). A poly mask is laid down (207) to define the CMOS gates and the word lines of the array after which, the standard CMOS flow is followed (step 208).

[0085] In the first embodiment, the deep boron concentration is reduced by counter doping. In this embodiment, shown schematically in Fig. 9, to which reference is now made, a double pocket is produced with Boron (210) and Arsenic or Phosphorous (212). The process is similar to that shown in Fig. 8, except that there are two pocket implant steps. The Boron is implanted first, using the dosage, energy and angles described hereinabove, after which the Arsenic or Phosphorous is implanted. The dosage for the Arsenic is $5x10^{13}$ per cm^2 at 180Kev and at an angle of 15° to the right and left of vertical.

[0086] The Arsenic or Phosphorous, being n+, cancels the affect of the Boron (which is p-) deep in substrate 105. To aid the primary injection, the Boron remains present near the surface, but little Boron, if any, is present deep in substrate 105 where secondary electrons are produced.

[0087] In an alternative embodiment, illustrated in Figs. 10A, 10B and 10C to which reference is now made, the surface of the channel is enhanced. This improves the primary injection mechanism without improving the secondary injection mechanism. Thus, programming will take less time (due to the improved primary mechanism) and less secondary electrons will be injected. Furthermore, the deep Boron concentration is reduced with respect to the prior art.

[0088] The surface enhancement is provided, in Fig. 10A, by a shallow threshold voltage Vt implant 220 of Boron. The cell can be produced without a pocket (Figs. 10A and 10B) or with a pocket (Fig. 10C). Fig. 10B shows a double threshold voltage implant. The remaining elements are the same as in previous embodiments.

[0089] Threshold voltage Vt implant 220 is produced after the low voltage gate oxide growth step (step 205). To create it, a shallow implant mask, defining the locations of implant 220, is first laid down, after which Boron of 3 - $5x10^{12}$ per cm^2 at 25Kev and at an angle of 7° parallel to the shallow implant mask is implanted. If the cell is produced without pockets (as in Figs. 10A and 10B), then step 193 is not performed. Otherwise (for Fig. 10C), it is performed.

[0090] Threshold voltage Vt implant 220 is a shallow implant since it occurs at the end of the high temperature processes and thus, does not have much chance to diffuse into channel 100. The result is an implant that is more concentrated near a surface 221 of channel 100. The implant is less concentrated further into substrate 105. For example, the concentration is typically reduced by a factor of 2 at a distance of 50 - 100nm from

surface 221. It will be appreciated that the distance from surface 221 at which the Boron is significantly reduced is a function of the size of the cell and will be reduced as the cell gets smaller. Thus, shorter distances of even 10nm are possible.

[0091] Fig. 10B illustrates an alternative version of this embodiment with two threshold voltage Vt implants. The first implant is a shallow implant of Boron, as in the previous embodiment. However, the second implant, labeled 230, is a deep implant of Arsenic or Phosphorous. This counterdoping ensures that the Boron implant extends only to a known depth.

[0092] To manufacture such a cell, two implant operations occur using the shallow implant mask. The first implant is of Boron, as described hereinabove. The second implant, of Arsenic or Phosphorous, is of 1 - $1.5x10^{12}$ per cm^2 at 90Kev or 45Kev, respectively, and at an angle of 7° parallel to the shallow implant mask.

[0093] A further embodiment, shown in Fig. 10C, adds Boron pockets 222 to shallow implant 220. In this embodiment, shallow implant 220 provides the desired surface concentration. Boron pockets 222 add to the surface concentration and provide Boron somewhat deeper into substrate 105. However, since shallow implant 220 provides the desired surface concentration, the Boron concentration can be reduced, to at least half that of the previous pockets. Thus, the deep concentration of Boron is minimal.

[0094] To produce the embodiment of Fig. 10C, the Boron pocket implants (step 193) are of 0.4 - $0.75x10^{13}$ per cm^2 (as opposed to $1.5x10^{13}$ per cm^2) at 60Kev and at an angle of 25° to the right and left of vertical. The shallow implant 220 (after step 205) is Boron of 1 - $2.5x10^{12}$ per cm^2 (as opposed to the 3 - $5 x10^{12}$ per cm^2 of previous embodiments) at 25Kev and at an angle of 7° parallel to the shallow implant mask.

[0095] Reference is now made to Figs. 11A and 11B, which illustrate further embodiments of the present invention having a deeper junction and a shorter channel length L_{eff}, respectively. Both features can be implemented separately, if desired or in combination.

[0096] In Fig. 11A, the bit lines, here labeled 102' and 104', are shown extending further into substrate 105 than in the previous embodiments. This can be produced through longer oxidation periods, during which the bit lines diffuse into substrate 105 in all directions. This includes diffusing toward each other and deeper into substrate 105.

[0097] It will be appreciated that the deeper junctions of Fig. 11A collect most of the secondary electrons before they get to the surface. This is indicated by arrows 230. Thus, fewer secondary electrons will be injected into nitride layer 110.

[0098] In Fig. 11B, the channel width, marked by L'_{eff}, is shorter than it is in the previous embodiments (it is marked in Fig. 11A by L_{eff}). A shorter channel has a larger lateral field, for the same drain to source voltage V_{ds}, and thus, the primary injection is increased, without increasing the secondary generation. Alternatively, for the same lateral field, the drain to source voltage V_{ds} can be reduced. The primary injection remains the same but the secondary generation is reduced.

[0099] Furthermore, a depletion region, such as the one marked 232, around the drain 104 further reduces the size of the channel during programming or reading. Most of the secondary electrons will be injected into drain 104 or its depletion region 232, as indicated by arrows 234, rather than into nitride layer 110. Thus, the shorter channel reduces the probability T of injection into nitride layer 110.

[0100] The methods and apparatus disclosed herein have been described without reference to specific hardware or software. Rather, the methods and apparatus have been described in a manner sufficient to enable persons of ordinary skill in the art to readily adapt commercially available hardware and software as may be needed to reduce any of the embodiments of the present invention to practice without undue experimentation and using conventional techniques.

[0101] It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described herein above. Rather the scope of the invention is defined by the claims that follow:

Claims

1. A method of creating a nitride, programmable read only memory (NROM) cell, the method comprising the step of:

   decoupling injection of channel hot electrons into a charge trapping layer of said NROM cell from injection of non-channel electrons into said charge trapping layer.

2. A method according to claim 1 wherein said step of decoupling includes the step of minimizing the injection of said non-channel electrons into said charge trapping layer.

3. A method according to claim 1 wherein said step of decoupling includes the step of minimizing the generation of said non-channel electrons.

4. A method according to claim 2 wherein said step of injection minimization includes the step of minimizing the concentration of Boron deep in the substrate.

5. A method according to claim 4 wherein said NROM cell has at least Boron pocket implants and wherein said step of Boron concentration minimization includes the step of implanting pocket implants of one of Arsenic and Phosphorous deeper than said Boron pocket implants.

6. A method according to claim 2 and wherein said step of injection minimization includes the step of implanting a shallow threshold voltage implant.

7. A method according to claim 6 and wherein said threshold voltage implant step includes the step of implanting two threshold voltage implants, a first surface implant of Boron and a second deeper implant of one of Arsenic and Phosphorous.

8. A method according to claim 6 and including the step of implanting Boron pockets.

9. A method according to claim 2 and wherein said step of injection minimization includes the step of implanting deep bit lines.

10. A method according to claim 2 wherein said NROM cell has a channel and wherein said step of injection minimization includes the step of making said channel to be shorter than a standard length.

11. A method according to claim 10 and wherein said step of injection minimization also includes the step of implanting deep bit lines.

12. A method according to claim 3 wherein said step of generation minimization includes the step of minimizing the concentration of Boron deep in the substrate.

13. A method according to claim 12 wherein said NROM cell has at least Boron pocket implants and wherein said step of Boron concentration minimization includes the step of implanting pocket implants of one of Arsenic and Phosphorous deeper than said Boron pocket implants.

14. A method according to claim 3 and wherein said step of generation minimization includes the step of implanting a shallow threshold voltage implant.

15. A method according to claim 14 and wherein said threshold voltage implant step includes the step of implanting two threshold voltage implants, a first surface implant of Boron and a second deeper implant of one of Arsenic and Phosphorous.

16. A method according to claim 14 and including the step of implanting Boron pockets.

17. A method according to claim 3 wherein said NROM cell has a channel and wherein said step of generation minimization includes the step of making said channel to be shorter than a standard length.

18. An NROM cell comprising:

a substrate having two bit lines and a channel therebetween;

an ONO layer at least above said channel; and

a shallow threshold voltage implant at least of Boron into said channel.

19. An NROM cell according to claim 18 wherein the concentration of said Boron is reduced by a factor of 2 at at least a distance of 10 - 20nm from a surface of said channel.

20. An NROM cell according to claim 18 wherein the concentration of said Boron is reduced by a factor of 2 at at least a distance of 20 - 30nm from a surface of said channel.

21. An NROM cell according to claim 18 wherein the concentration of said Boron is reduced by a factor of 2 at at least a distance of 30 - 40nm from a surface of said channel.

22. An NROM cell according to claim 18 wherein the concentration of said Boron is reduced by a factor of 2 at at least a distance of 40 - 50nm from a surface of said channel.

23. An NROM cell according to claim 18 wherein the concentration of said Boron is reduced by a factor of 2 at at least a distance of 50 - 100nm from a surface of said channel.

24. A cell according to claim 18 and wherein said shallow threshold implant has a first implant of Boron and a counterdoping implant of one of Arsenic and Phosphorous, wherein said counterdoping implant is deeper in said channel than said first implant.

25. A cell according to claim 18 and also comprising a pocket implant near at least one of said bit lines.

26. An NROM cell comprising:

a substrate having two bit lines and a channel therebetween;

an ONO layer at least above said channel; and

a double pocket implant near at least one of said bit lines wherein said double pocket implant is formed of two pocket implants, a p+ implant near a surface of said substrate and an n-implant below said p+ implant.

27. An NROM cell comprising:

a substrate having two bit lines and a channel therebetween, wherein said channel is no longer than 0.2μm wide; and

an ONO layer at least above said channel.

28. An NROM cell according to claim 27 and wherein said channel is no longer than 0.15μm wide.

29. An NROM cell according to claim 27 and wherein said channel is no longer than 0.1μm wide.

30. An NROM cell comprising:

a substrate having two bit lines and a channel therebetween, wherein said bit lines have a depth of no less than 0.3μm into said substrate; and

an ONO layer at least above said channel.

31. An NROM cell according to claim 30 wherein said channel is no longer than 0.2μm wide.

32. An NROM cell according to claim 30 and wherein said channel is no longer than 0.15μm wide.

33. An NROM cell according to claim 30 and wherein said channel is no longer than 0.1μm wide.

34. A method of creating a nitride, programmable read only memory (NROM) cell, the method comprising the step of:

having a high ratio of surface injection to deep injection of electrons into a charge trapping layer of said NROM cell.

35. A method according to claim 34 wherein said NROM cell has at least Boron pocket implants and wherein said step of having includes the step of implanting pocket implants of one of Arsenic and Phosphorous deeper than said Boron pocket implants.

36. A method according to claim 34 and wherein said step of having includes the step of implanting a shallow threshold voltage implant.

37. A method according to claim 36 and wherein said threshold voltage implant step includes the step of implanting two threshold voltage implants, a first surface implant of Boron and a second deeper implant of one of Arsenic and Phosphorous.

38. A method according to claim 36 and including the step of implanting Boron pockets.

39. A method of creating a nitride, programmable read only memory (NROM) cell, the method comprising the step of:

generating a zero substrate potential at a distance no less than 45 - 55nm into said substrate.

40. A method according to claim 39 wherein said step of generation includes the step of minimizing the concentration of Boron deep in the substrate.

41. A method according to claim 40 wherein said NROM cell has at least Boron pocket implants and wherein said step of Boron concentration minimization includes the step of implanting pocket implants of one of Arsenic and Phosphorous deeper than said Boron pocket implants.

42. A method according to claim 39 and wherein said step of generation includes the step of implanting a shallow threshold voltage implant.

43. A method according to claim 42 and wherein said threshold voltage implant step includes the step of implanting two threshold voltage implants, a first surface implant of Boron and a second deeper implant of one of Arsenic and Phosphorous.

44. A method according to claim 42 and including the step of implanting Boron pockets.

45. A method according to claim 39 wherein said NROM cell has a channel and wherein said step of generation includes the step of making said channel to be shorter than a standard length.

46. A method of operating a nitride, programmable read only memory (NROM) cell to have minimum injection from non-channel electrons, the cell having bit lines serving as source and drain to said cell, the method comprising the step of:

providing the lowest source voltage Vs which provides a desired drain to source voltage V_{ds} to said cell.

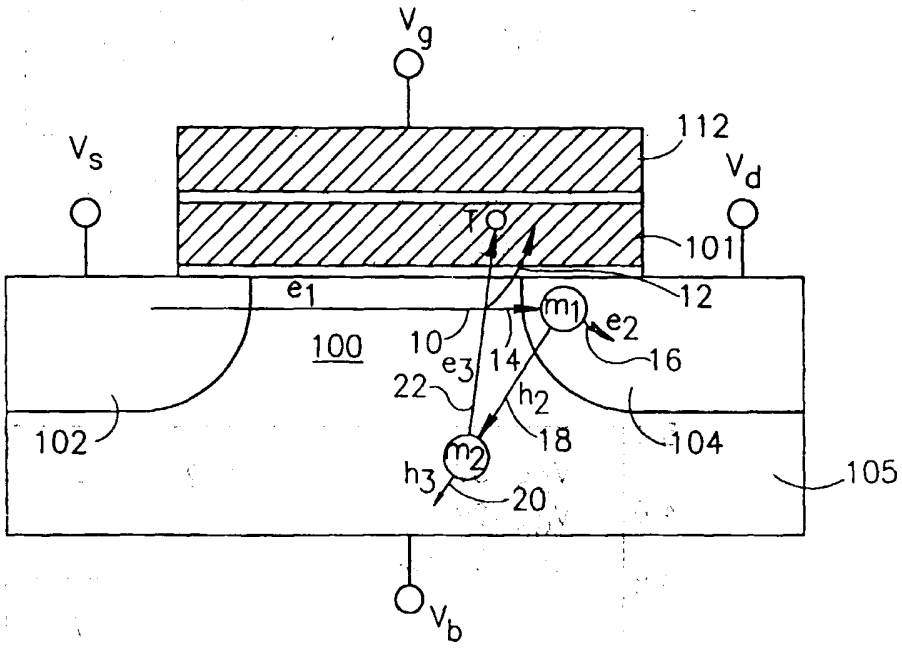

FIG.1
PRIOR ART

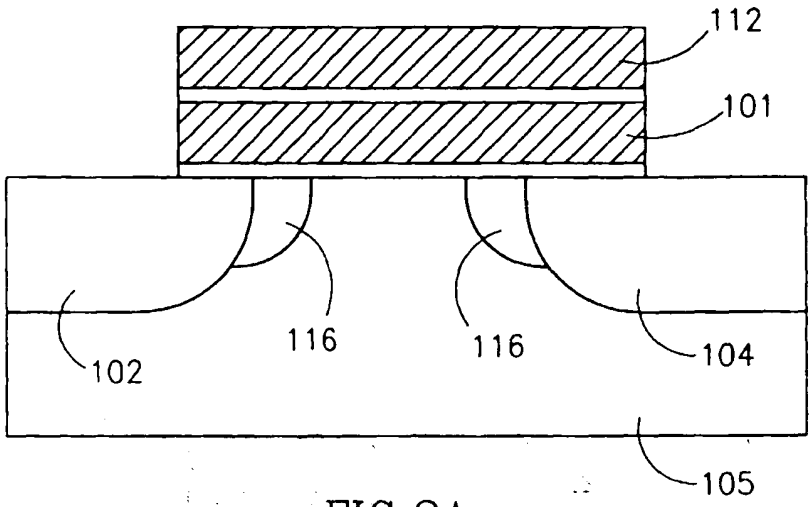

FIG.2A
PRIOR ART

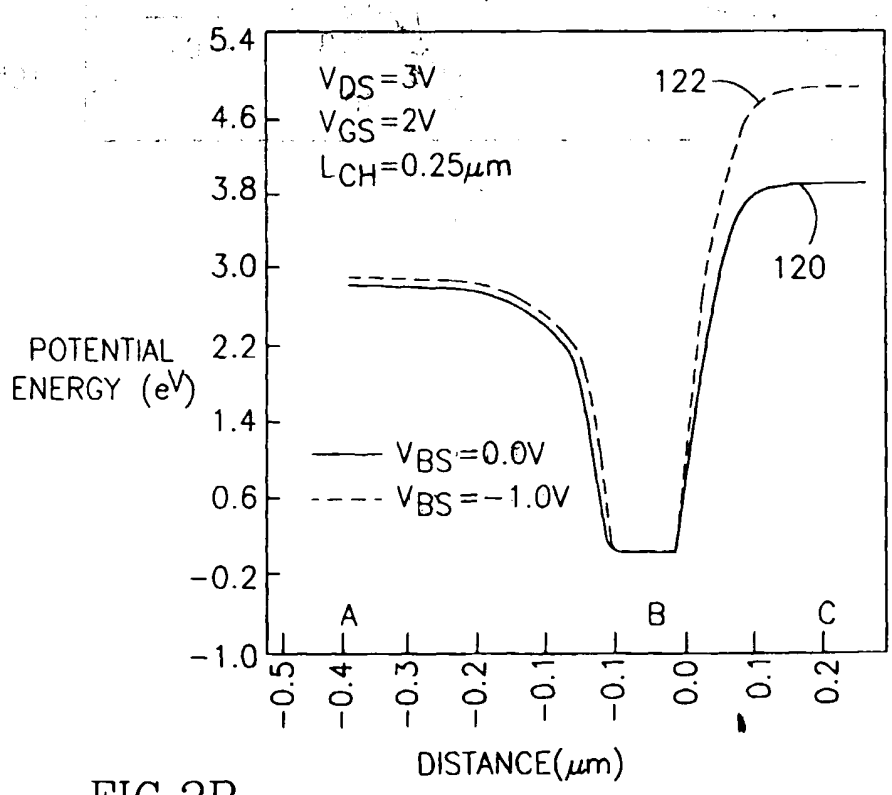

FIG.2B

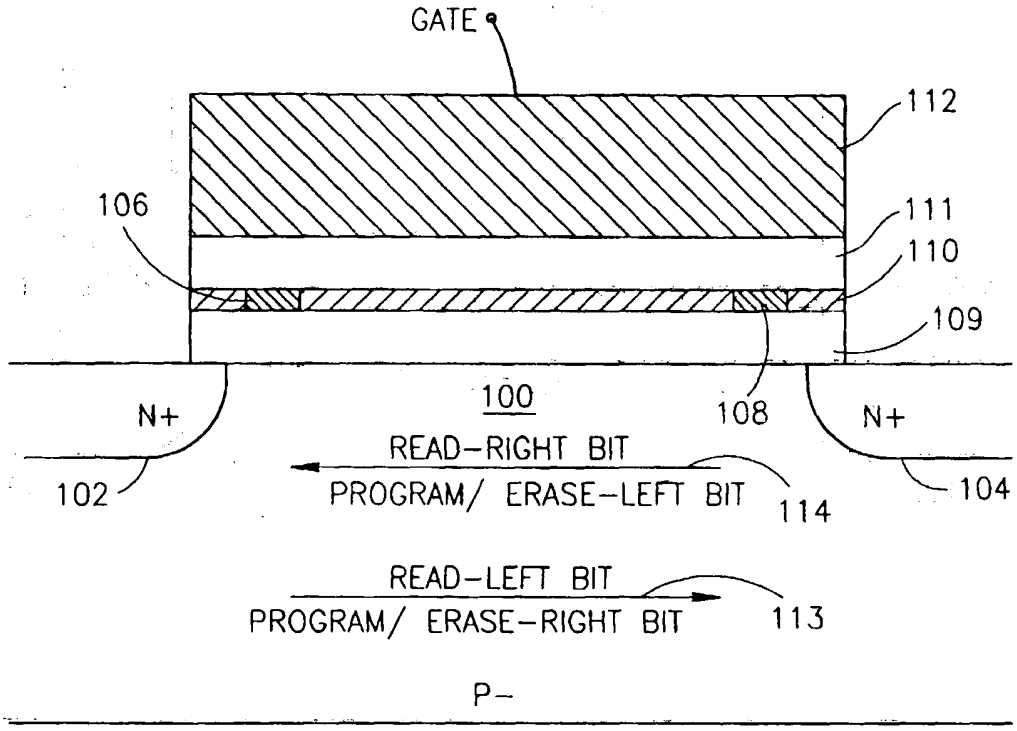

FIG.3A
PRIOR ART

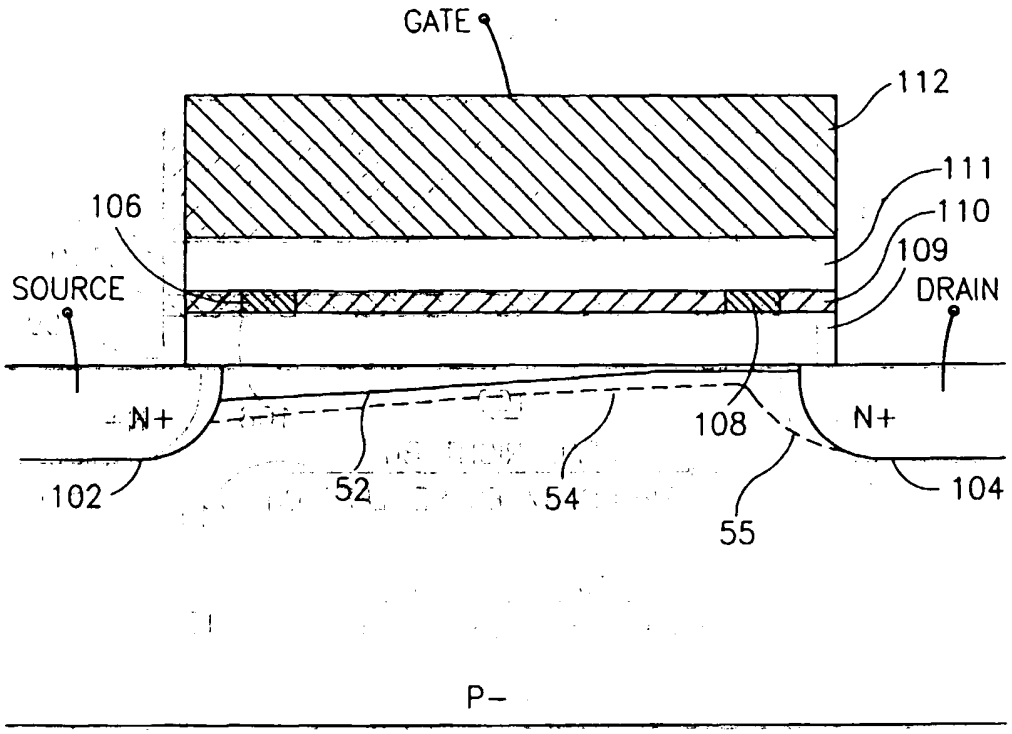

FIG.3B
PRIOR ART

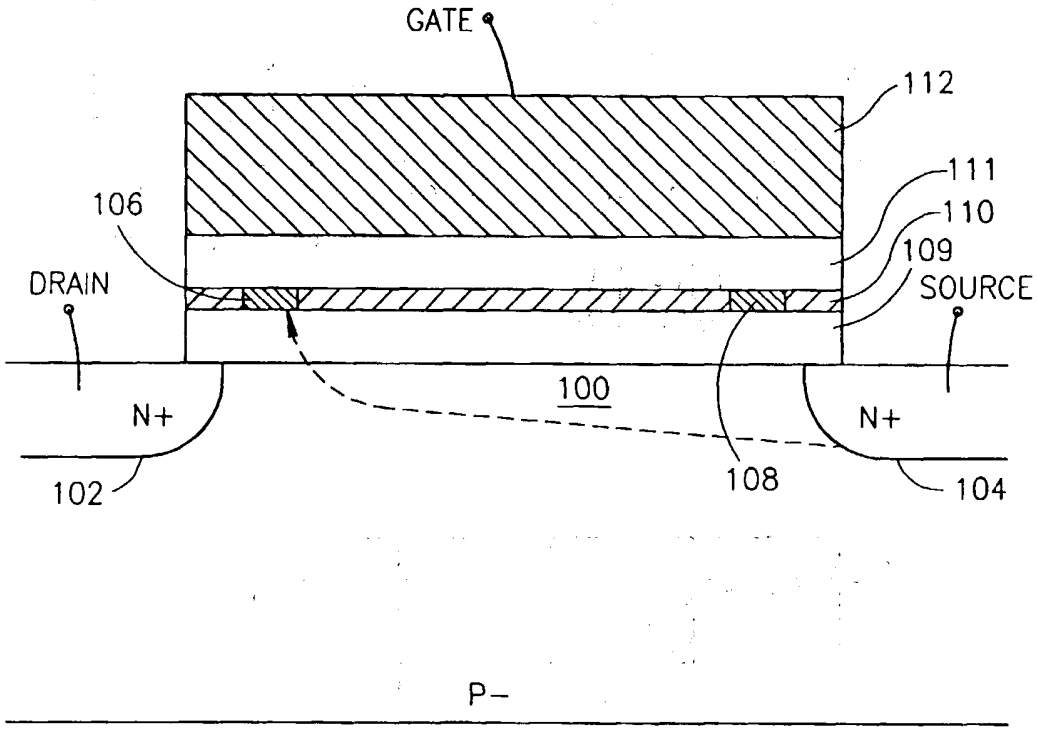

FIG.3C
PRIOR ART

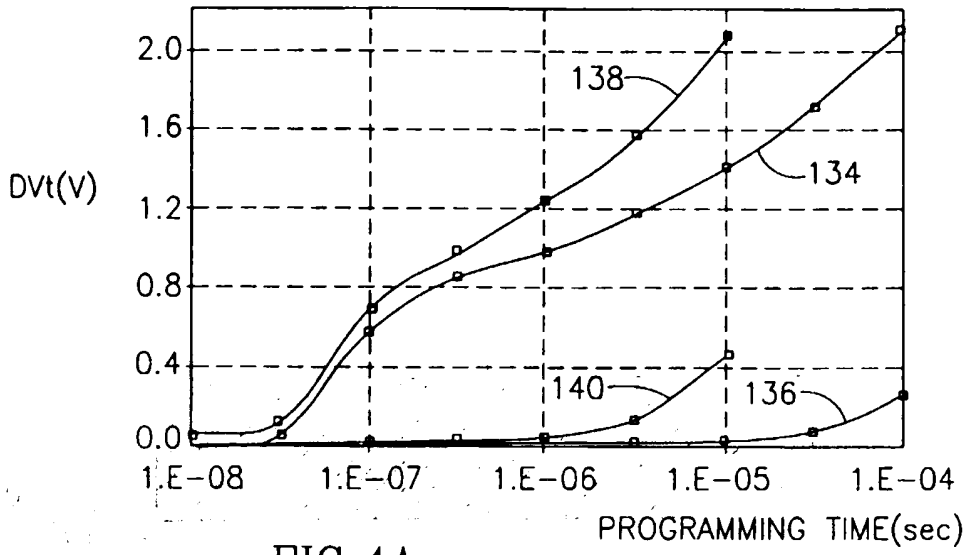

FIG.4A
PRIOR ART

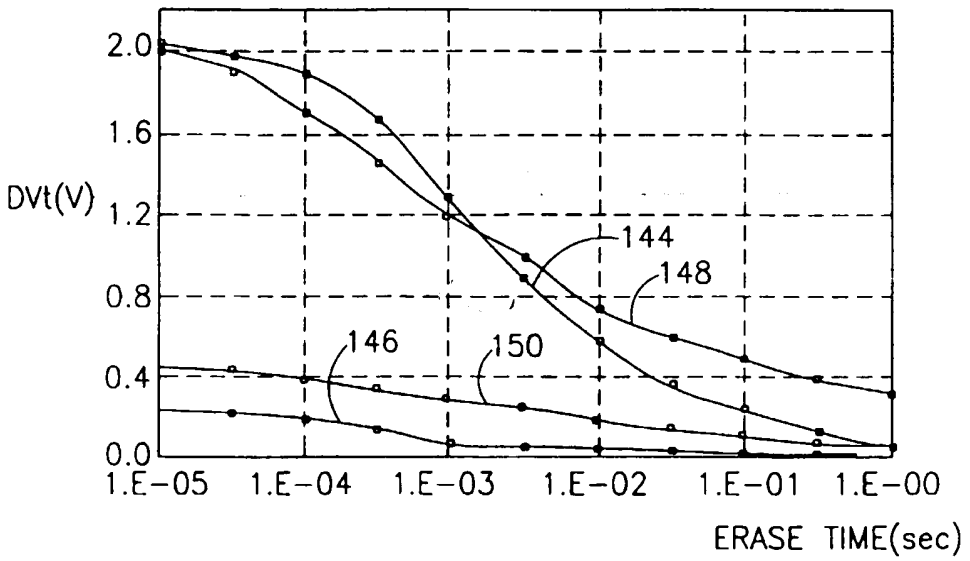

FIG.4B
PRIOR ART

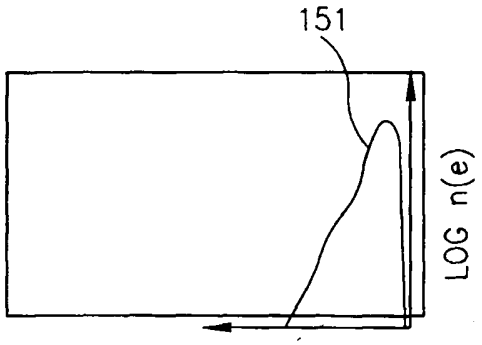

FIG.5A
PRIOR ART

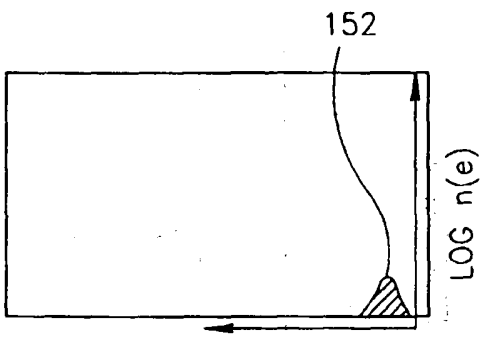

FIG.5B
PRIOR ART

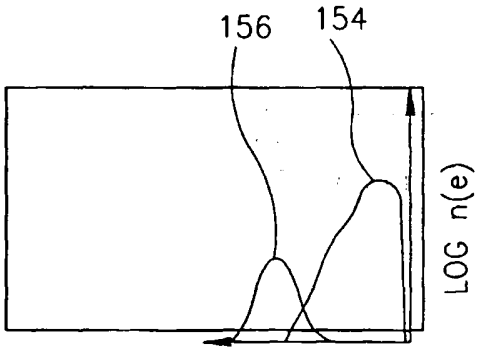

FIG.5C
PRIOR ART

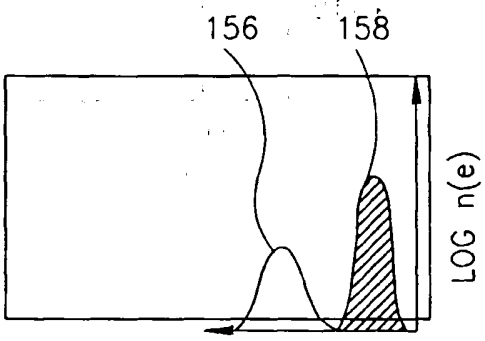

FIG.5D
PRIOR ART

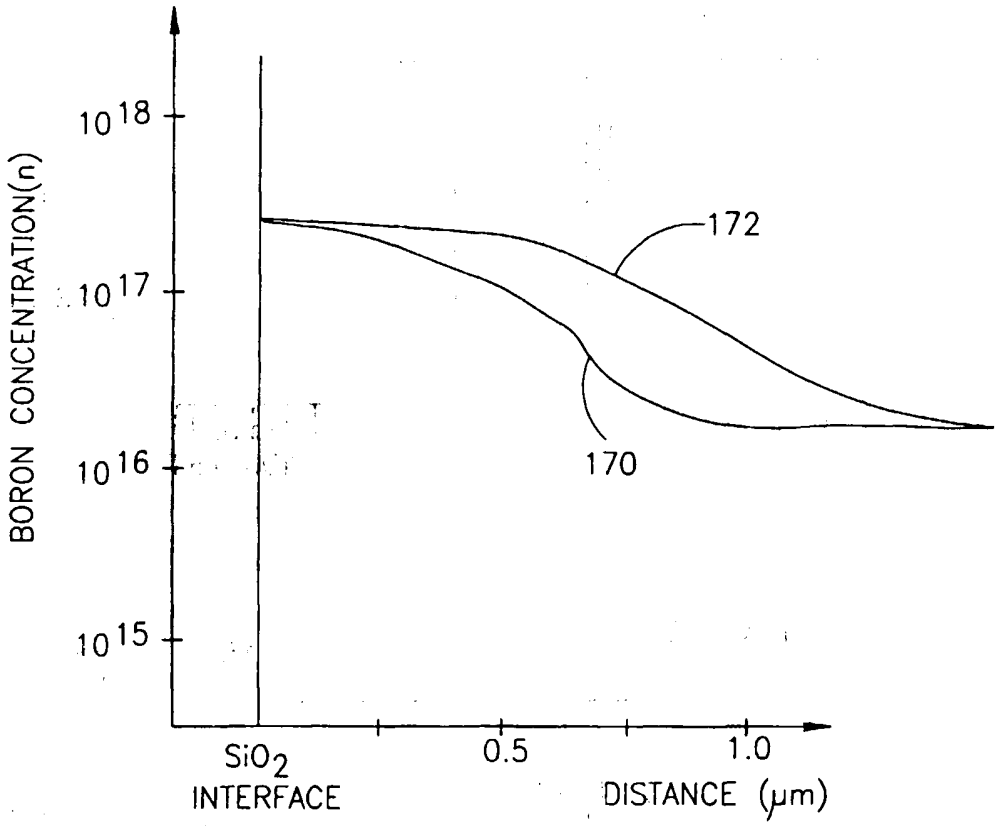
BORON CONCENTRATION(n)
10^{18}
10^{17}
10^{16}
10^{15}
172
170
SiO_2
INTERFACE
0.5
1.0
DISTANCE (μm)

FIG.6A

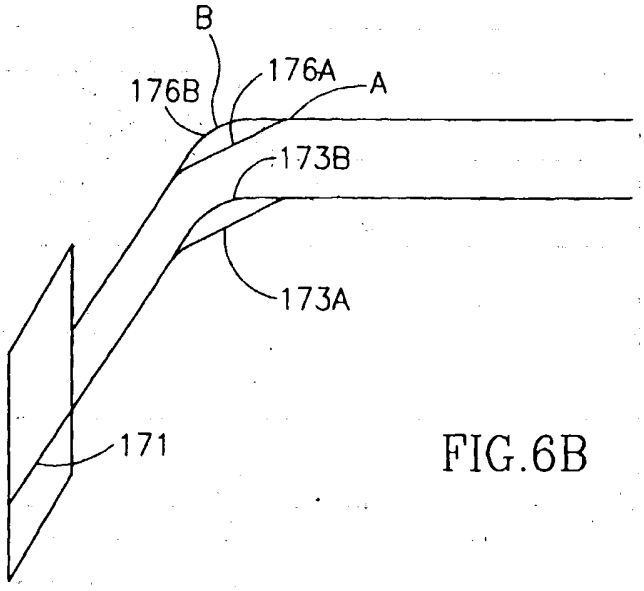

FIG.6B

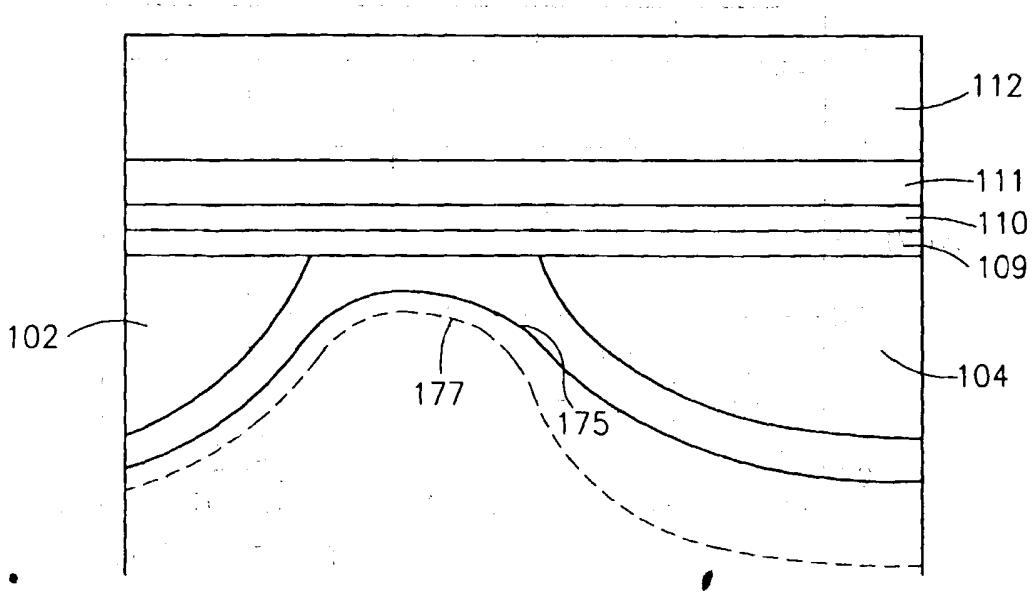

FIG.6C

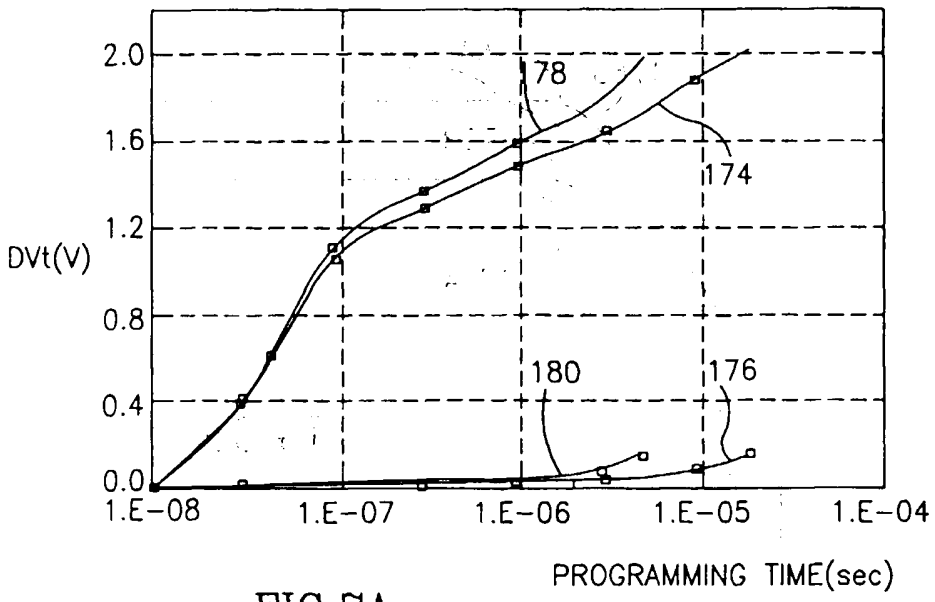
2.0
1.6
1.2
0.8
0.4
0.0
DVt(V)
78
174
180
176
1.E-08
1.E-07
1.E-06
1.E-05
1.E-04
PROGRAMMING TIME(sec)

FIG.7A

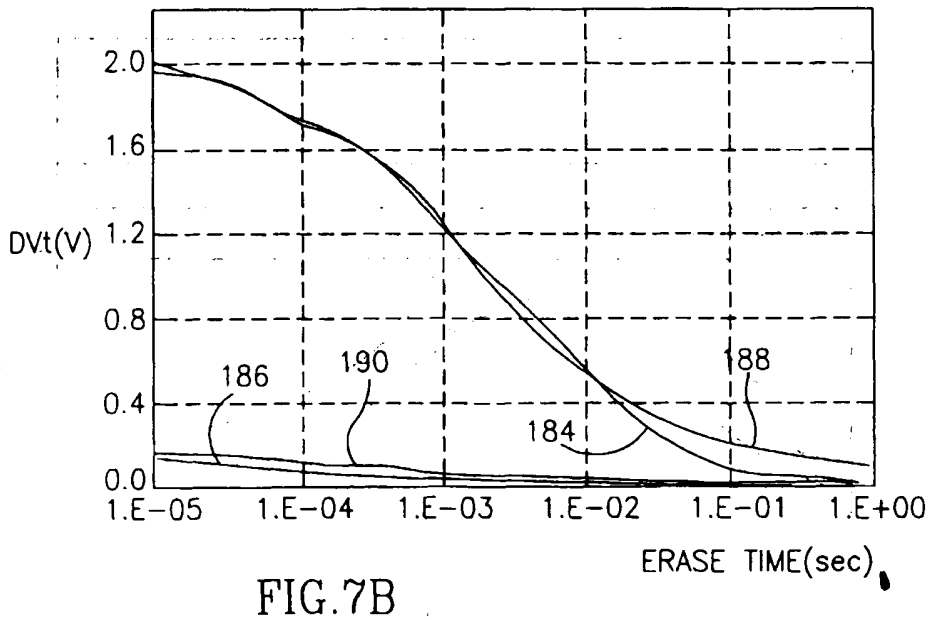
2.0
1.6
1.2
0.8
0.4
0.0
DVt(V)
186
190
188
184
1.E-05
1.E-04
1.E-03
1.E-02
1.E-01
1.E+00
ERASE TIME(sec)

FIG.7B

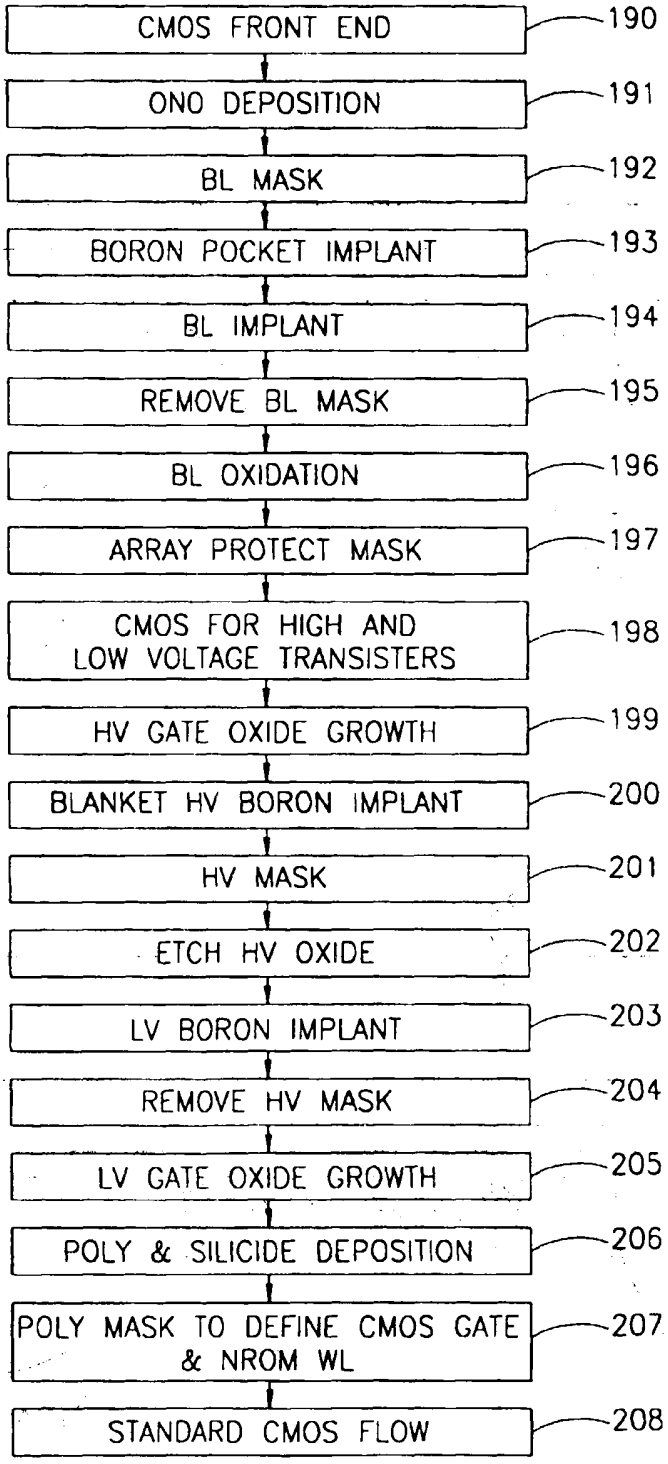
CMOS FRONT END
190
ONO DEPOSITION
191
BL MASK
192
BORON POCKET IMPLANT
193
BL IMPLANT
194
REMOVE BL MASK
195
BL OXIDATION
196
ARRAY PROTECT MASK
197
CMOS FOR HIGH AND LOW VOLTAGE TRANSISTERS
198
HV GATE OXIDE GROWTH
199
BLANKET HV BORON IMPLANT
200
HV MASK
201
ETCH HV OXIDE
202
LV BORON IMPLANT
203
REMOVE HV MASK
204
LV GATE OXIDE GROWTH
205
POLY & SILICIDE DEPOSITION
206
POLY MASK TO DEFINE CMOS GATE & NROM WL
207
STANDARD CMOS FLOW
208

FIG.8

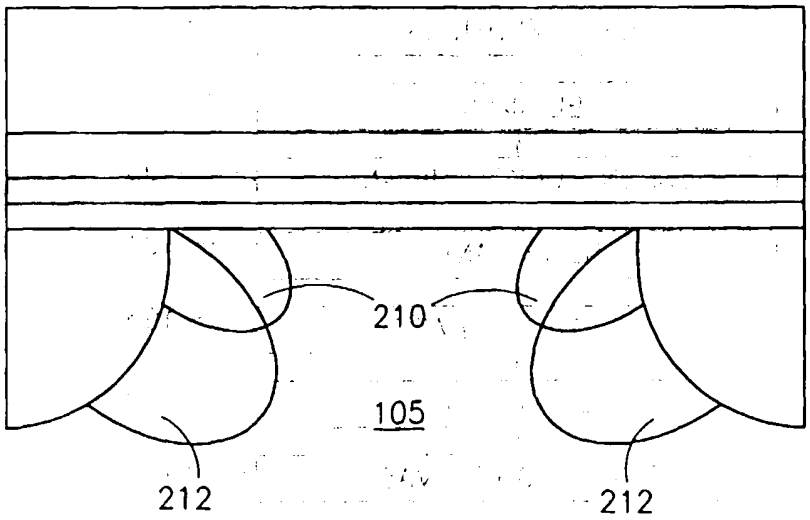

FIG.9

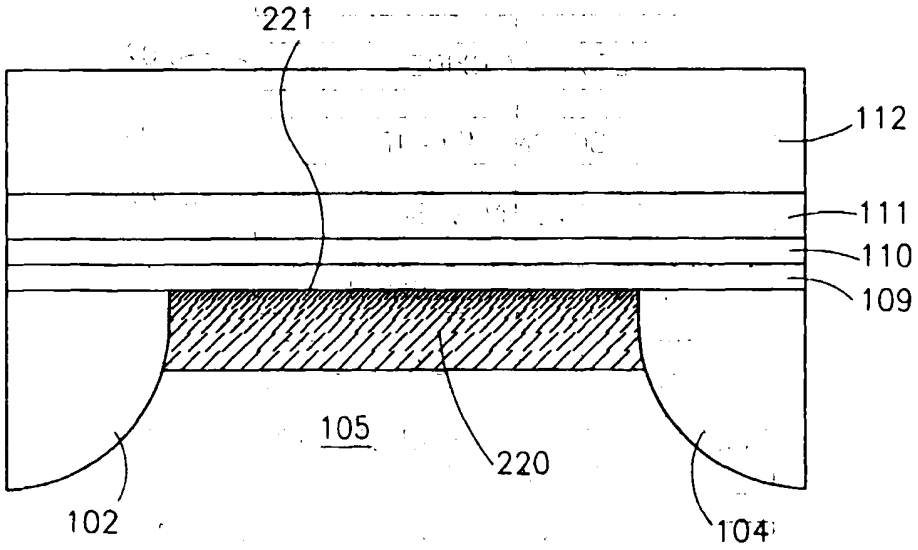

FIG.10A

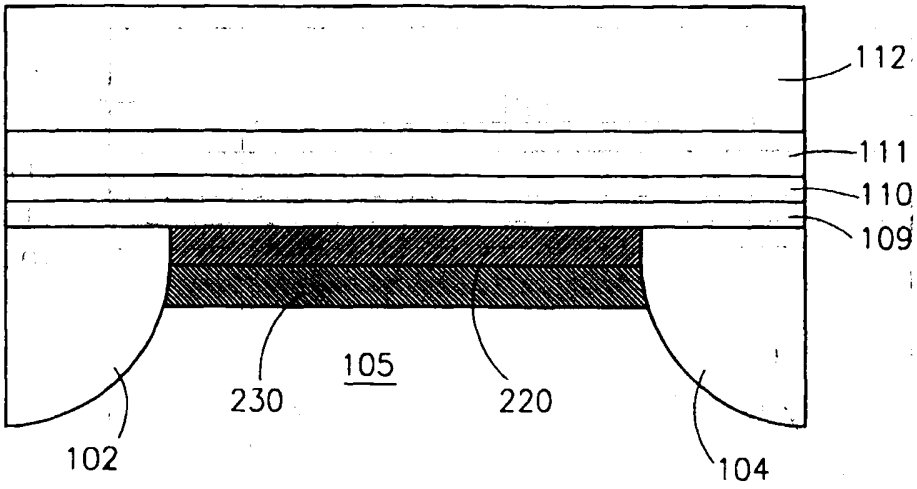

FIG.10B

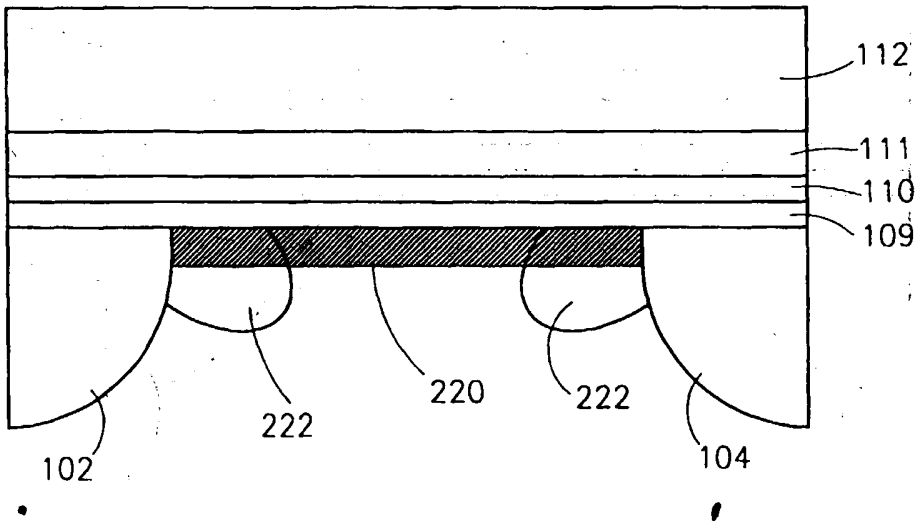

FIG.10C

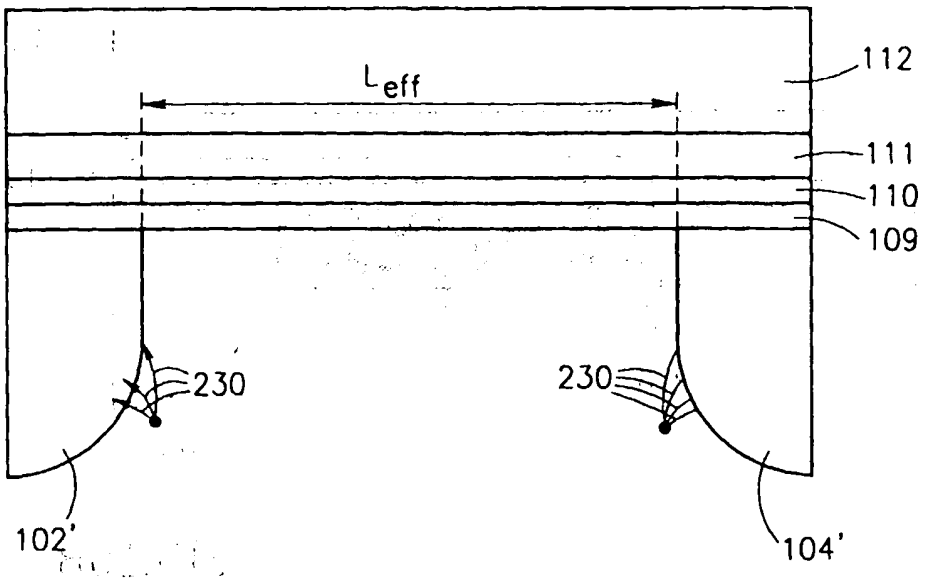

FIG.11A

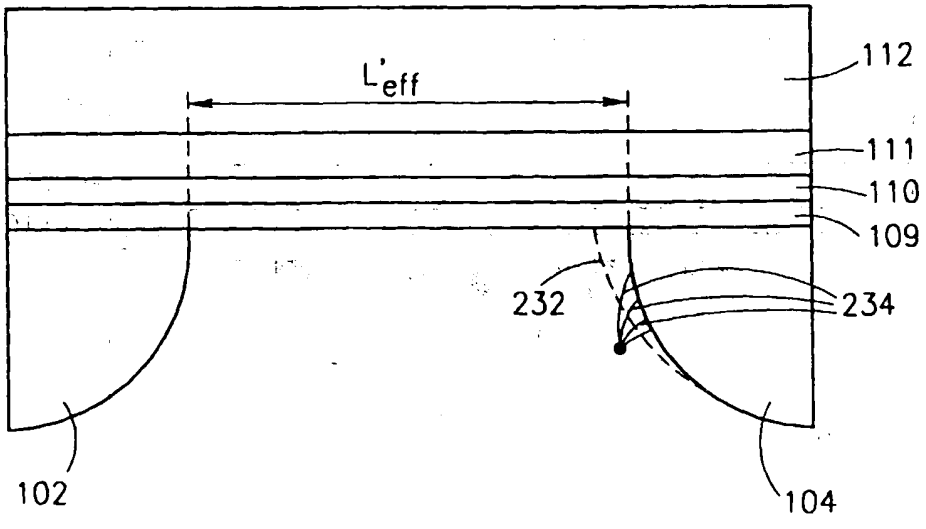

FIG.11B

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EUROPEAN SEARCH REPORT

Application Number
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	23 February 2001	Lindquist, J

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